REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-76 remain in the application. Claims 1-38 are subject to examination and claims 39-76 have been withdrawn from examination. Claims 1 and 20 have been amended. Claims 77 and 78 have been canceled.

In item 3 on page 2 of the above-identified Office Action, claims 1-7, 10-11, 13-26, 29-30, 32-38, 77, and 78 have been rejected as being anticipated by Moore et al. (U.S. 6,598,148) (hereinafter "Moore") under 35 U.S.C. § 102(e).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found in the previously presented claims.

More specifically, the features added to independent claims 1 and 20 relate, inter alia, to the structural hardware unit being configured for access to the memory device independently of the intelligent core.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a program-controlled unit, having:

an intelligent core configured to process instructions to be executed;

a structurable hardware unit selectively forming an application-specifically configurable intelligent interface for respectively connecting the intelligent core and the units, including **an interface connection between the intelligent core and the internal peripheral units, between the intelligent core and the external peripheral units, between the intelligent core and the memory devices, and between the plurality of units;**

the structurable hardware unit having direct connections and configurable data paths and data linkage paths between devices to be connected by the structurable hardware unit and being configured for access to the memory devices independently of the intelligent core and for evaluating and processing data and signals received thereby, the structurable hardware unit including a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal

The Moore reference discloses a microprocessor integrated circuit having a processing unit located on an integrated circuit substrate. The processing unit operates according to a predefined set of program instructions which are stored in an instruction register. The integrated circuit also has a memory for storing information provided by the processing unit. The substrate also has a ring oscillator thereon. The microprocessor 50 multiplexes the address/data bus by using a feedback to allow the processor to adjust memory bus timing to be fast with small loads and slower with large loads. The output enable line 152 from the microprocessor 50 is connected to all the memories 150 on the circuit board and the loading on the enable line 152 to the microprocessor 50 is directly related to the number of memories 150 connected. The microprocessor monitors how rapidly line 152 goes high after a read and thus, is able to determine when the data hold time has been satisfied and place the next address on the bus. The microprocessor generates the system clock and clock circuit 430 tests process performance. The clock is disposed on the same chip as the microprocessor. There is no apparent disclosure in Moore of the interface connection between the intelligent core (shown as microprocessor 11 in the present application) and the various internal and external peripheral units and the memory devices with the structurable hardware unit (shown as SLE layer 12 in the present application) being

configured to access the memory devices independently of the core. It is not at all apparent from the disclosure in Moore that there is an independent access as recited in the instant claims. According to the present invention, the layer 12 can transfer data from and to the memory devices independently, that is, without the participation of the microprocessor, which is not shown in Moore.

Moore does not show "an interface connection between said intelligent core and said internal peripheral units, between said intelligent core and said external peripheral units, between said intelligent core and said memory devices, and between said plurality of units; said structurable hardware unit...and being configured for access to said memory devices independently of said intelligent core and for evaluating and processing data and signals received thereby, said structurable hardware unit including a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal" as recited in claim 1 of the instant application. Independent claim 20 contains similar limitations.

In item 24 on page 9 of the above-identified Office Action, claims 8, 9, 12, 27, 28, and 31 have been rejected as being

unpatentable over Moore in view of Takahashi et al. (U.S. 5,825,878) (hereinafter "Takahashi") under 35 U.S.C. § 103(a).

The foregoing discussion of Moore is equally applicable in this rejection.

Takahashi discloses a secure embedded memory management unit for a microprocessor for data transfer from an external memory. While Takahashi shows the use of NAND gates 56, 60, there is no apparent reason why one skilled in the art would necessarily combine Takahashi with Moore other than through hindsight. There is no teaching or suggestion in Moore that Moore requires or for that matter would even want to use the NANDs shown in Takahashi. And even if the combination of Takahashi with Moore is proper, which it is not, the resulting unit still would not result in the claimed invention. Takahashi does not overcome the deficiencies of Moore.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1 or 20. Claims 1 and 20 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 20.

In view of the foregoing, reconsideration and allowance of claims 39-76 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for reply is required, petition for extension is herewith made.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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FDP/bb

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